

Module 4B7: VLSI Design, Technology, and CAD

Laboratory Experiment

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Scanning Electron Microscopical Examination of CMOS Integrated Circuit

Name

College

Date

This coursework counts for 25% of the available credit for the module. Please make the report at most **four** pages long. You may include extra pages of data, graphs and images above the total. Hand in your report and this experiment sheet to the cabinet outside the EIETL by 5pm on Monday, 2nd May 2011. Late reports will incur a penalty and in extreme cases may not be marked.

1. Introduction

In this experiment you will use a scanning electron microscope as a tool to examine small structures including CMOS devices for VLSI circuits. During the session the group will record some images, which you can view or process digitally in the DPO or elsewhere and include in your report. Please share the images as a group, but select and discuss them independently as you prepare your individual write-up. Any of the resources handed out during the 4B7 module can be used/annotated and included in your write-up. Include in your account the WWW addresses of any sites or links you find useful during your preparation. We will also provide an interactive virtual SEM, which you can access by means of a web browser to carry out certain parts of the experiment.

Some of the points mentioned below will come out naturally during the course of the session; in other case you will need to ask questions or research topics elsewhere.

In the write-up, we would like you to:

- Outline briefly the electron sources available for scanning electron microscopes and the compromises in terms of resolution and magnification obtainable, ease of use, lifetime, and cost.
- Explain the significance of the excitation voltage used for SEM of integrated circuits in relation to the type of formation that can be obtained from the resulting images.
- Briefly compare and contrast scanning electron microscopy with optical microscopy and other microscopical techniques of which you are ware for inspection of advanced CMOS circuits.
- Measure the actual dimensions of the NOR gates on the specimen CMOS chip, the pitch of the polysilicon interconnect in the 2-input NOR gate, and the total process bias in micrometres per edge on the Al metal 1 layer. Note that the dimensions used on the CAD system employed for the design were in units of whole micrometres.
- Label the salient features of Fig. 6, and shade in the active gate regions of the transistors.
- One of the circuits on the chip is a divide-by-two CMOS circuit containing six logic gates. Include in the write-up a circuit diagram and explanation of the circuit operation.

There are more details about the above in later sections. Some additional objectives:

- Study the input and output bond pads and supporting circuitry, and obtain images of any other features that capture your interest.
- Use the SEM to study the Si- micromachined pits close to the exposed NOR gates on the specimen CMOS chip. How would you go about estimating their depth using the SEM? How accurate would you expect this to be?

2. The Scanning Electron Microscope

Figure 1 shows a schematic electron column, controls and display. The sample is bombarded with electrons in a vacuum. The electron probe is scanned across a portion of the sample in raster fashion to build up a picture. Figure 2 illustrates some possible approaches to examining samples with electron beams. A more detailed diagram showing the structure of the column is shown overleaf, in Fig 3.

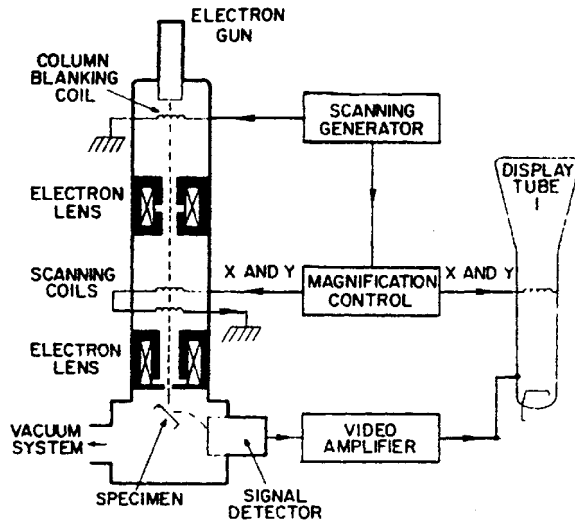


Fig 1 - General arrangement of the SEM

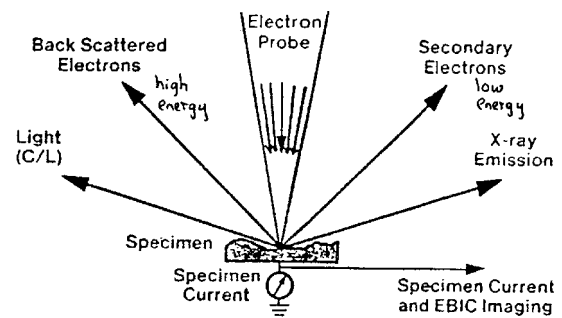


Fig 2 - Imaging modes of the SEM

In today's experiments, the signal consists of **secondary electrons**, which are emitted from the sample surface. Contrast is mainly from variations in the sample topography i.e. the local angles between the normal to the surface and the incident electron beam and the secondary electron collector. Resolution is determined by the spot size of the electron probe, possibly less than 5 nm.

Back-scattered electrons which have high energy comparable with the primary beam (e.g. 40 keV) may also be used to form an image which is less sensitive to topology and more sensitive to variations in the atomic mass across the sample than is the secondary image.

Light emission (cathodoluminescence) or **X-ray emission** giving information about chemical composition may also be used to image the sample.

Principles of Operation

Electrons are emitted from a hot filament electron gun at high negative potential with respect to the grounded anode. They travel along the column to the specimen, which is mounted on a micrometer-controlled stage.

Magnetic condenser lenses focus the electron beam to a spot on the surface of the specimen. This spot is scanned across the sample in raster fashion using scanning coils which deflect the beam in x and y.

Secondary electrons emitted from the sample are attracted to the collector screen, which is at a positive potential. Most of the electrons pass through the screen and are further accelerated on to the scintillator (e.g. at +10 kV) where they produce photons.

In the photomultiplier the photons are absorbed by a photo-emissive surface, which again produces electrons. The electron current is amplified by cascading the electrons down a series of collectors each of which produces more secondary electrons, i.e. *secondary electron multiplication*.

The resultant video signal is used to modulate the electron beam on the display cathode ray tube to produce a magnified image of the surface.

The electron energy - which is adjustable - determines how far the electron probe penetrates the sample. Samples (particularly biological specimens) are often coated with a metal to make the surface conducting and avoid charging effects during observation. Low energy beams (a few kV) may be used to investigate insulating surfaces (e.g. passivated integrated circuits and devices), but with poorer resolution than is obtainable with higher energy beams.

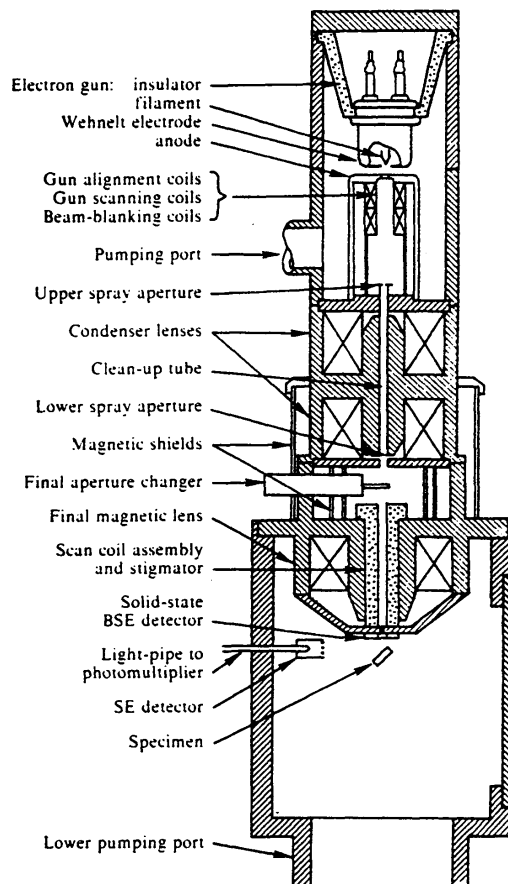


Figure 3 - Details of the SEM column

3. The Cambridge Virtual SEM (VSEM)

The Virtual SEM is a software tool designed as a training and reference resource for novice and experienced users of the Scanning Electron Microscope. A web-based environment delivers training modules on elements of SEM science and operating theory, as well as an encyclopaedia of SEM information and a SEM simulator. More information about the project is available on the web, at: www.virtualsem.com/about.php.

A version of the system has been developed specially for the Module 4B7 practical. You can access this at: www.virtualsem.com/moodle/. We will assign you a username and password for this during the practical session. The 4B7 practical content is found under the CUED course category.

We strongly encourage you to make use of this resource and to fill in the feedback questionnaire available at: www.virtualsem.com/4b7/survey.php.

Using the VSEM Simulator in the Practical Write-up

You will find the VSEM simulator useful as you gather material for your write-up:

Measurement of Device Dimensions: as in a real SEM, the VSEM simulator provides the ability to make measurements of features on the sample. Sample #1 in the simulator shows the area of the chip over which the top layer of passivation has been removed. Use this to measure the minimum fabricated polysilicon dimension.

Examination of Device Features: sample #2 in the simulator shows a low magnification view of the chip, including circuitry and bond pads.

Other samples are included in the simulator and may be used in your write-up should you wish.

4. SEM examination of silicon integrated circuits and other objects

The handout contains images of some of the objects you may observe, for purposes of orientation. **Please annotate the images during the session and attach the handout to your submitted report.**

Spend some time familiarising yourselves with the SEM control and specimen manipulation controls. Choose an object that interests you and centre it on the screen. Now start to increase the magnification. Use the focus, brightness and contrast level controls to obtain an optimum image. Many of these observations (but not all) can be repeated using the VSEM (Virtual SEM) – see below.

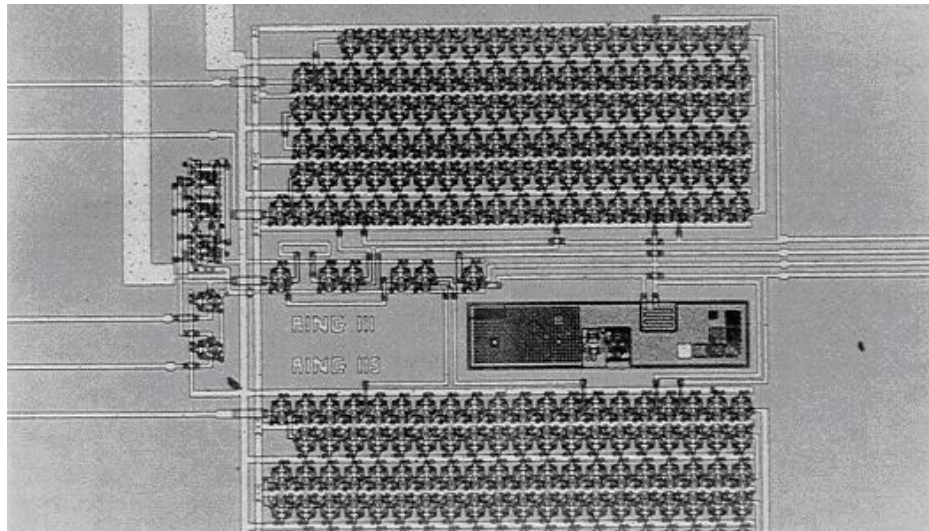


Fig. 4 – Overall view of ring oscillator specimen

An overall view of the chip under inspection is shown in the optical micrograph in Fig. 4. It contains a 111-stage ring oscillator with 2-input NOR gates. Figure 6 opposite shows an impression of the layout of the two input NOR gate used in its design. An optical micrograph of a similar chip is shown in Figure 7, and an X-Y scale is provided.

Identify and shade (i) the n-channel transistors (ii) the p-channel transistors in Figure 6.

Estimate the minimum linewidth designed for the polysilicon layer. Note that in this ring oscillator circuit all shapes are designed on a 1 μm grid, i.e. with dimensions in multiples of one micron.

Fig. 8 (a)-(c) is a series of SEM images of a single logic gate. In Fig. 8(a), **label the salient features, and shade in the active gate regions of the transistors.**

An SEM micrograph of an edge-triggered divide-by-two CMOS circuit is shown in Fig. 9 and the corresponding optical micrograph is in Fig. 10. It represents the structures found near $x = 5$ and $y = 50$ in Fig. 7. **Examine the structures carefully and identify the transistors and interconnections.** The corresponding circuit is given in Fig. 11.

There are test sites between the two ring oscillators where the top layer of passivation has been left out of the design. Locate these in the SEM image, and zoom in to see the structures in more detail (this experiment can also be carried out in VSEM). You will find 1-input and 2-input NOR gates in which successive layers have been omitted to show clearly the various layers in the device similar to Fig. 7 at $x = 100$ to 110, $y = 15$ to 20. Where the overlying metal 1 is left out, the polysilicon wiring is easily visible. **Investigate the structure of contacts, vias and other design features** that may be apparent. See also Figs. 8(b) and 8(c).

Try rotating the sample slowly (this needs to be done in the real SEM), and **observe the changes in contrast**, bearing in mind that the substrate holder is typically inclined at 30 degrees.

Figure 9 contains examples of artefacts commonly encountered in scanning electron microscopy. **Discuss the origin of these and identify examples of these appearing in your own images.**

Explore the device at low magnification, and **examine how the electrical connections are made to the outside world via bond pads.** You can repeat this experiment with VSEM.

5. Measuring actual device dimensions

In the deposition, lithographic and etch processes used in integrated circuit fabrication there are process biases which change the line widths and line separations from the original specifications, unless correct allowances are made for them by introducing *biases* on the masks. These fabrication tolerances are one of the major factors limiting the use of even smaller dimension devices in integrated circuits. You can measure the actual features on the ring-oscillator chip manufactured by European Silicon Structures (the silicon foundry responsible for its fabrication), compare them with the design and establish the net process biases on the corresponding layers, and the alignment accuracy between the mask levels. In some cases you may be surprised that the circuits work satisfactorily despite what you see in the SEM!

Calibration of the magnification of the scanning electron micrographs is very important and the sketch below shows one approach to length calibration that makes use of repeating structures on the chip.

It is based upon the assumption that the mask maker and the mask printer are good - i.e. the distance from the right hand side of one structure to the corresponding point on the right side of the next structure - is not changed in the process, even though line-widths generally are changed.

You should be able to verify this from your own observations with the SEM (or VSEM).

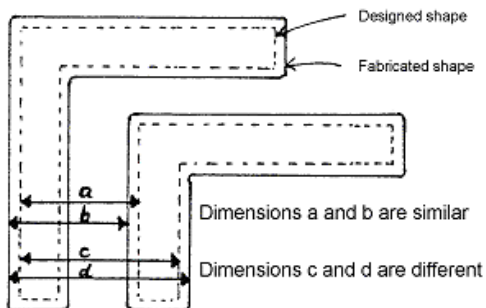


Fig. 5 – Process biases

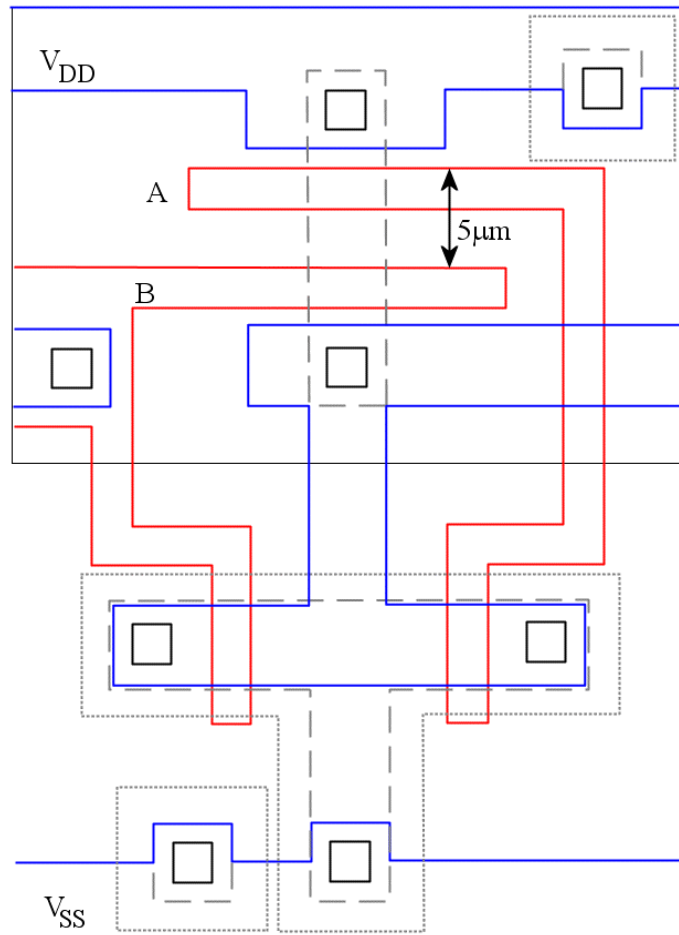


Fig 6 – Layout plot for NOR gate for Ring 111 & Ring 115

Determine the minimum polysilicon dimension fabricated, and attempt to compare this with the minimum *designed* dimension.

Explain how you would use a, b, c or d in the sketch (Fig. 5) to deduce the process bias.

The layout of the 2-input NOR gate in Fig. 6 shows the designed pitch between adjacent polysilicon interconnects.

6. Operating conditions

You are now free to follow up what most interests you. In your write-up, you should comment upon your investigations. Take and record the best quality micrograph you can of the 1- or 2- input NOR gates using the angle of specimen orientation that you find most clearly shows the structure of the devices. Try to identify the various features.

Note: We will upload saved images to a web site so you can access them after the session.

In your write-up, you should discuss the utility of SEM examination for CMOS and other devices, and any of the following phenomena:

Saturation: The brightness of the image does not increase if the filament current is increased beyond a certain point.

Astigmatism Correction: You will no doubt have observed that at high magnifications the image becomes difficult to focus. This can be partly due to the spot size of the focussed electron beam being too large, or due to astigmatism i.e. a non-circular beam shape. Correction for astigmatism can best be made by going to high magnification and focussing on a small round object. Then the astigmatism correction can be adjusted to obtain the sharpest possible image. In practice the focus and astigmatism should be optimised in an iterative way until no further improvement is possible.

Acceleration Voltage: Choose an interesting part of one of the specimens and make a sketch of a high-magnification image of it (so that you can recognise it again). Now vary the acceleration voltage between its present value of 40 kV and lower voltages such as 5 kV. Does the visibility of any surface structure in the image change with the acceleration voltage?

Charging Effects and Edge Effects: Find a feature with a sharp edge on one of the objects, use a medium acceleration voltage, and go to high magnification. The sharp edge should now appear as a bright line on the image i.e. an enhanced secondary electron signal or penetration fringe.

Include in your write-up any images your group has taken to illustrate these aspects of SEM behaviour, and label the main features.

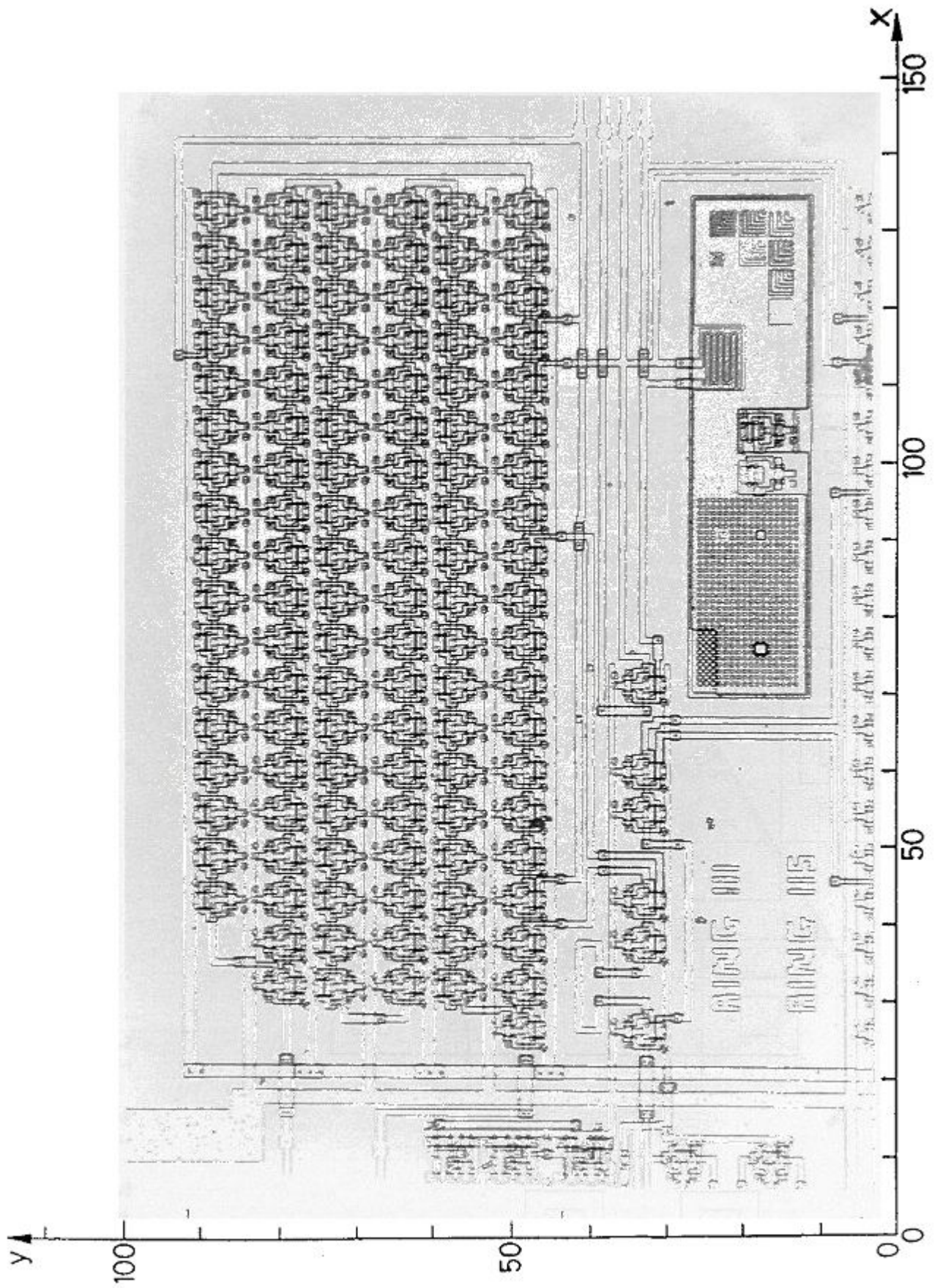


Figure 7 Ring 111/115 detail – optical micrograph

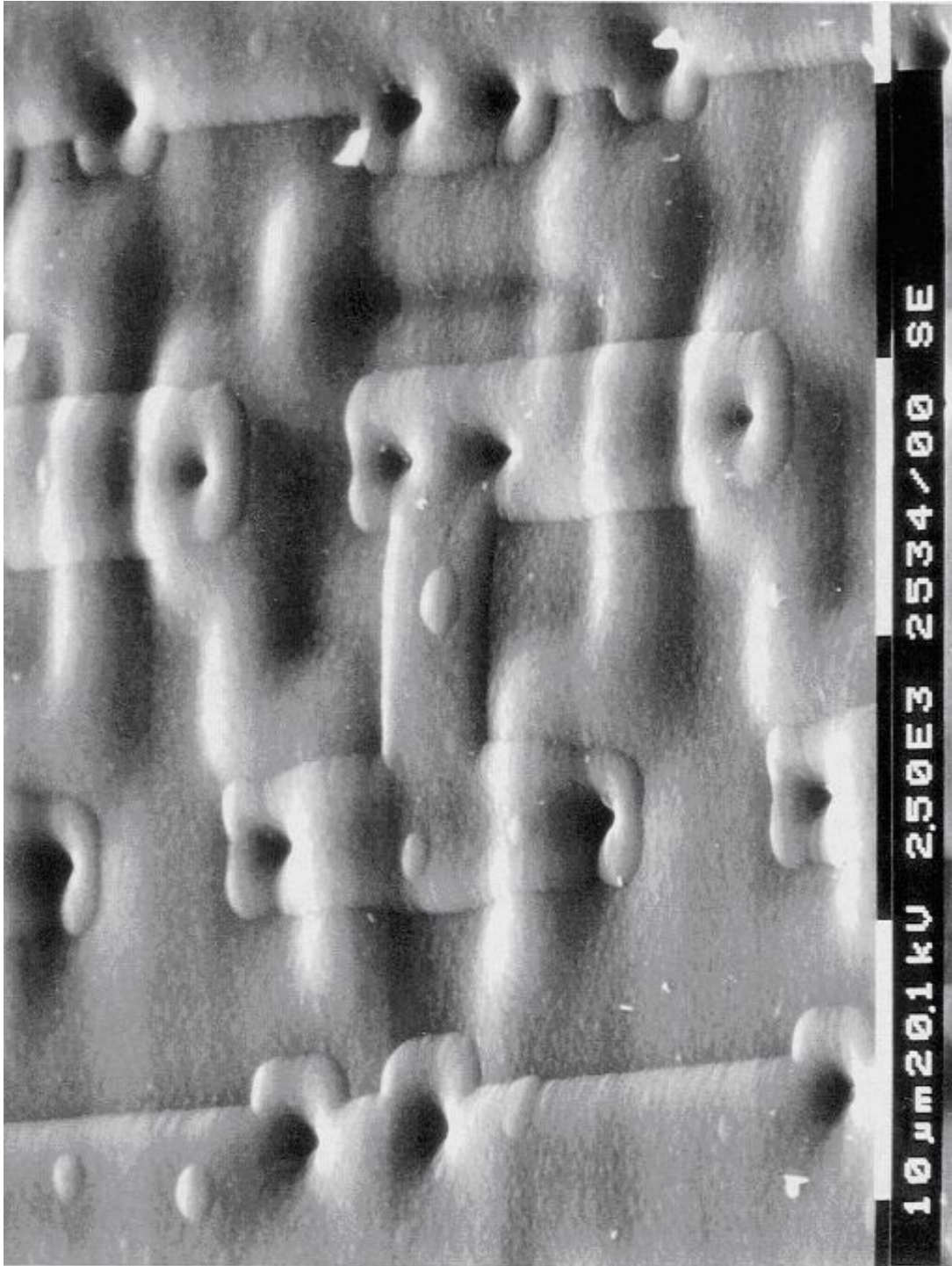


Figure 8(a) SEM image of part of the ring oscillator

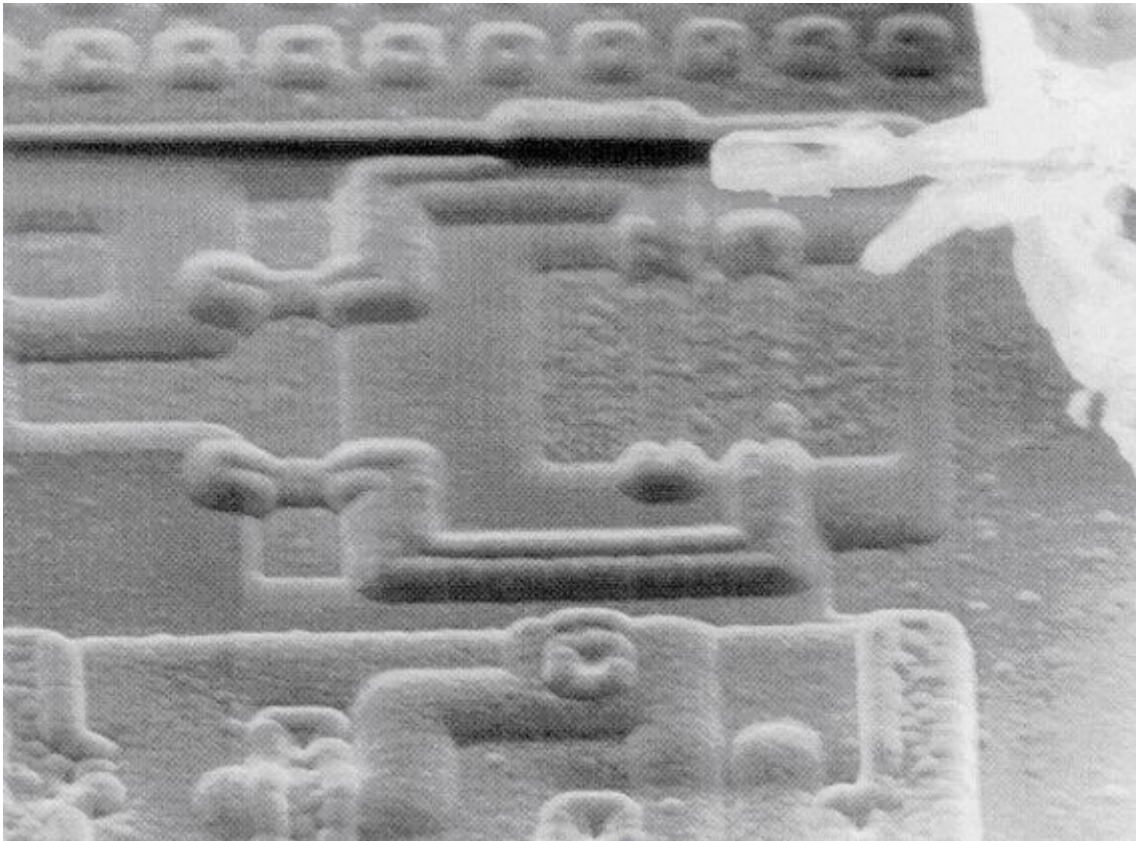


Figure 8(b)

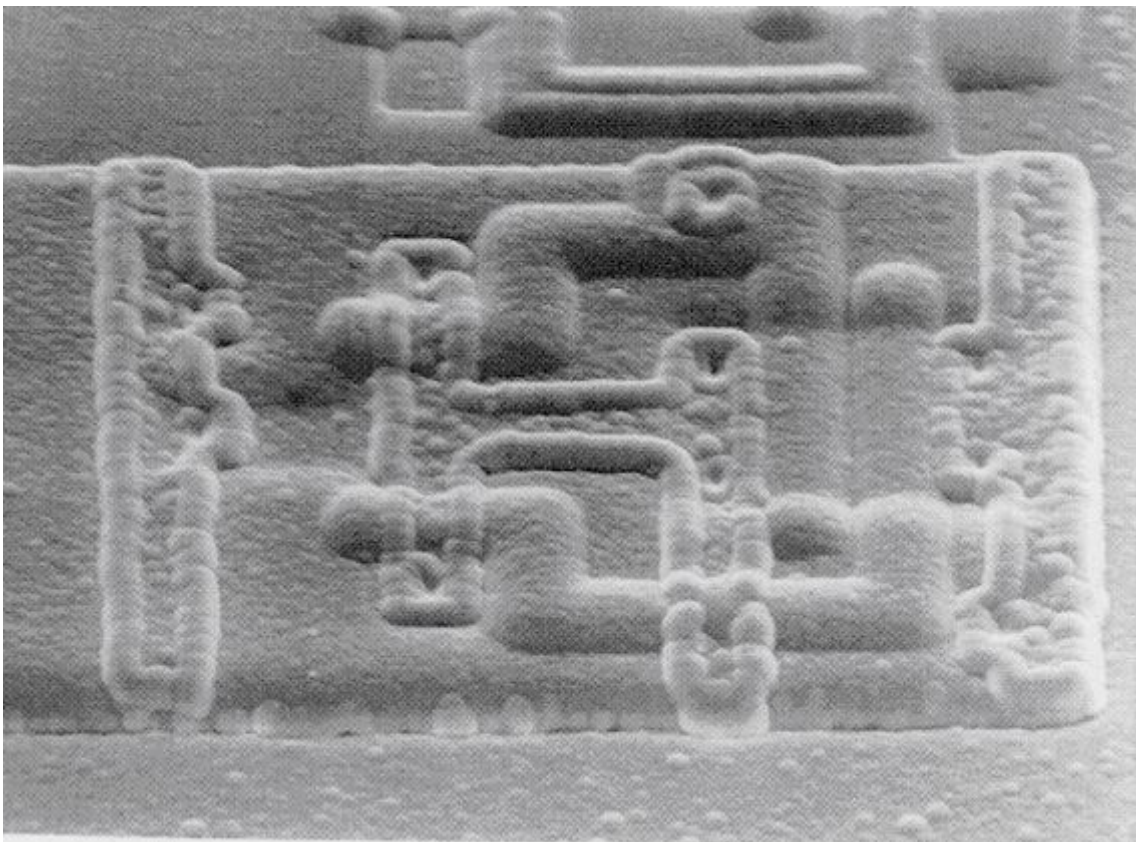


Figure 8(c)

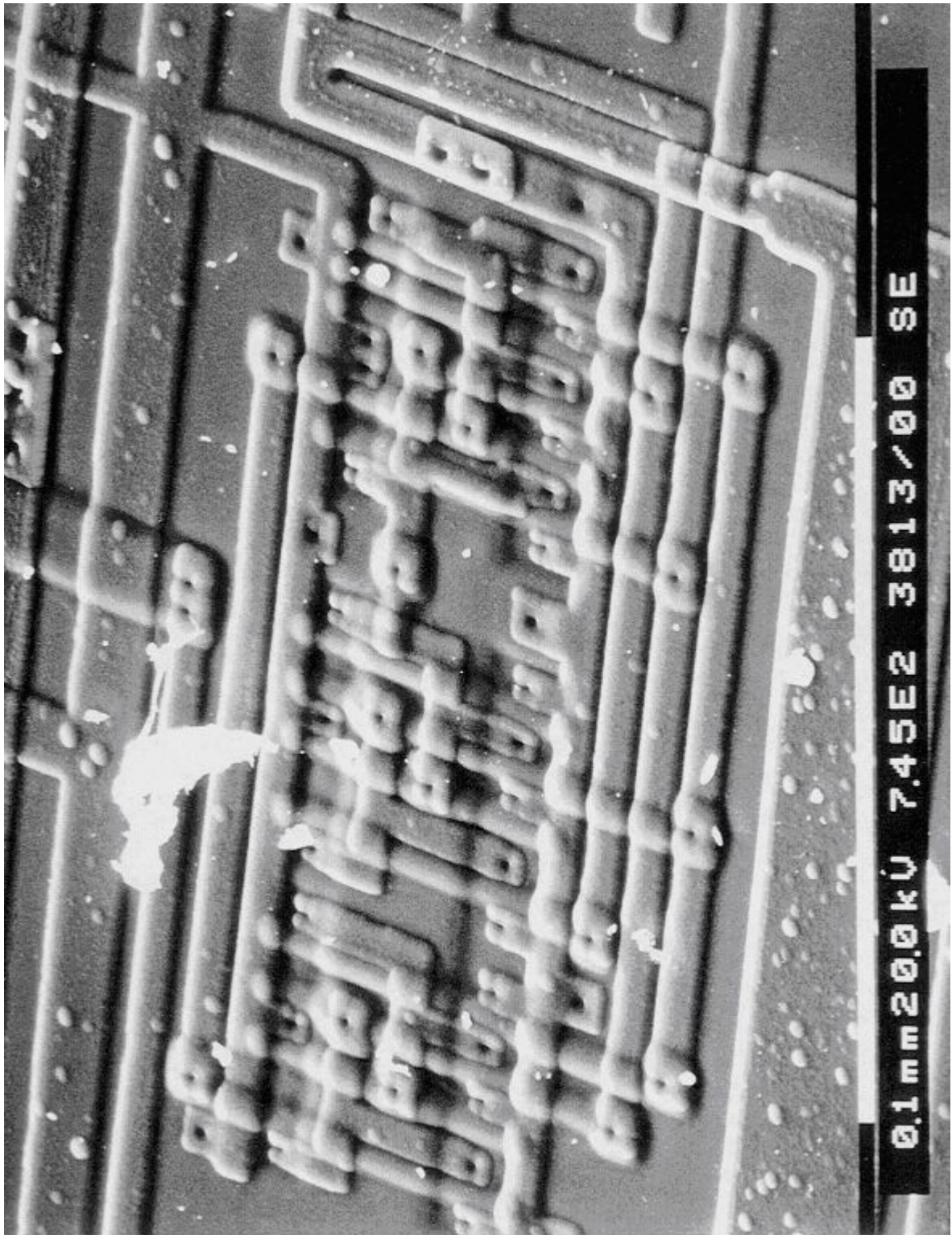


Figure 9

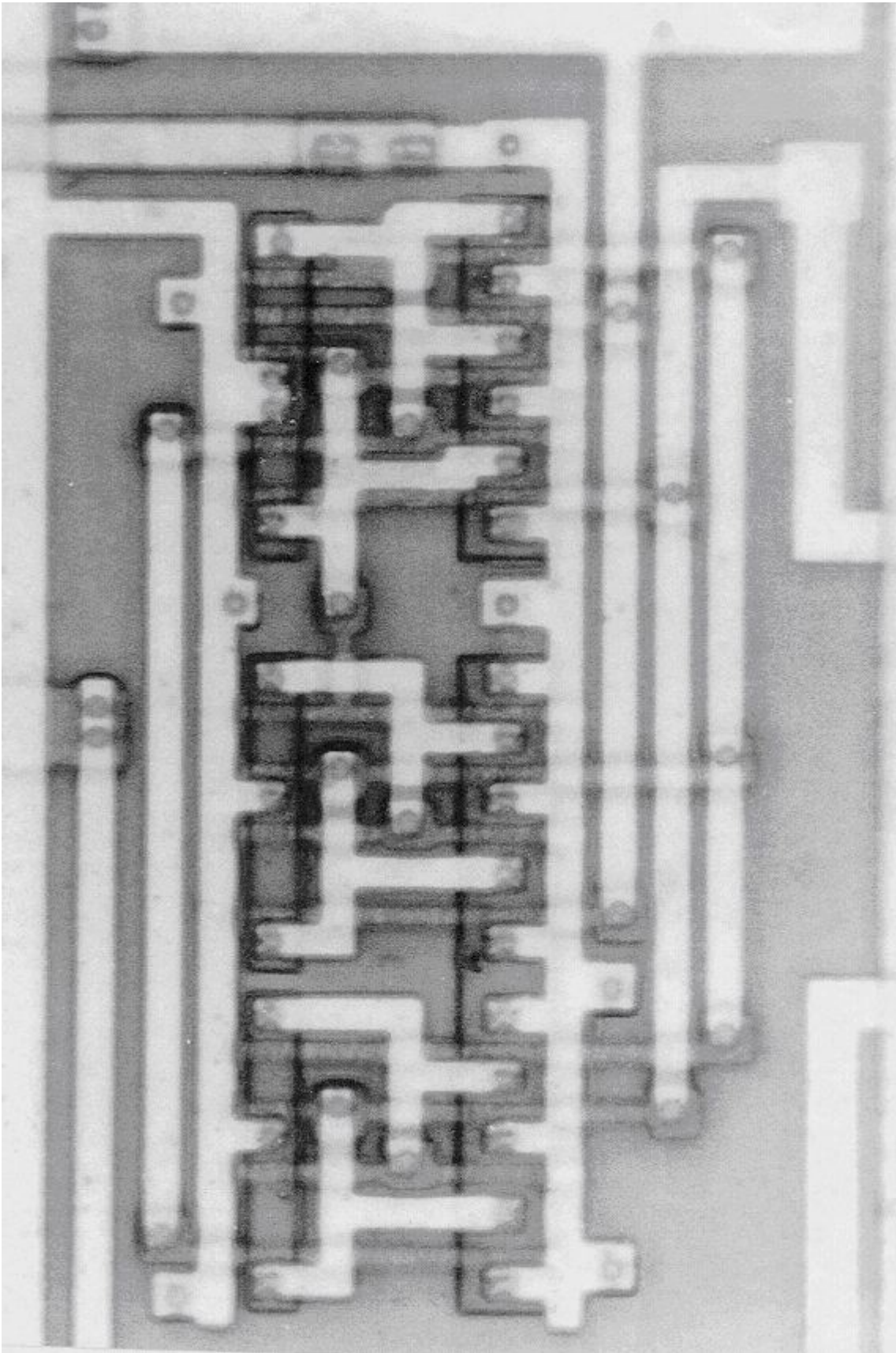


Figure 10

7. Appendix – Installation and Operation of the VSEM Simulator

Installation

The simulator can be run directly from its Java package without needing to install the simulator itself. However, it requires the latest Java runtime environment (JRE) to be installed on your computer for it to run. Java installation files are available from within the “Resources” section of the Module 4B7 course on the website.

Once you have installed the JRE, the following instructions will get you up and running with the simulator:

- Download “simulator.zip” from the 4B7 course area on the website
- Unpack this file in a convenient location (e.g. on the Desktop)
- Open the resulting folder and run (by double-clicking) vsem_sim.jar

Operation

When you run the simulator, two windows will open – one allows you to choose which sample to load and the other is the main simulator window.

To the right of the text area at the bottom of the simulator window is a button labelled “Help”. This is available at all times and will bring up a panel containing comprehensive instructions on how to use the software.

Hints:

- Change the setup of the simulator to suit you (this is done via the “Setup” button which is above the “Help” button)
- Image measurements may be made through the Image tab at the top right of the main simulator window – this tab will only become available once you have loaded a sample
- You may have to adjust the simulator settings (use the “Lenses / Stage” tab) before you can see the sample clearly enough to make measurements

Feedback

Please do let us have feedback on the VSEM software. A feedback survey is available at www.virtualsem.com/4b7/survey.php