Computer-Based Project in VLSI Design Co 3/8

Laboratory Guide 3 - Transistor schematics

This laboratory guide introduces the Mentor Graphics *Design Architect* application for the capture and manipulation of transistor level schematics. **Lab session 4**, which follows, will focus more directly on the use of *Design Architect* itself. Here we use the tool to investigate the transistor level schematic for the 2 input NOR gate, to be designed as a CMOS mask set, and explore some of the key constraints that govern the design procedure. The information gathered in this session forms an important part of the **First Interim Report**.

This lab session is divided into three sections.

Section I Familiarisation with *Design Architect*. Print out schematics.
Section II Determination of correct design parameters for transistors in **nor2t**.
Section III Adaptation of the **nor2t** schematic for use in later sessions.

Once you have investigated the transistor-level specification of the 2 input NOR gate and generated a printed copy of the schematic (Section I), a substantial part of the work covered in this guide can be completed off-line, away from the workstation. Only a brief session is required at the workstation in order to gather the necessary information.

You should be logged in at a workstation as described in the **Getting Started** chapter, with both *Design Manager* and *Design Architect* running, but with no schematic or symbol window open.

Section I - Familiarisation with Design Architect

1. Open the existing sheet **nor2t**.
   Click on the **OPEN SHEET** button in the palette window. The Open Sheet dialogue box appears.
   Fill in the Component Name box with: **$CBT_WD/nor2t**.
   Leave the sheet name as **sheet1** and OK the dialogue box.
   When the Edit window appears, study the resulting schematic. You should see wires and ports similar to those used in the schematics of earlier sessions, but notice that the components used are those corresponding to standard p-type and n-type MOS transistors rather than logic gates.

   You will find it useful to generate a printed copy of the schematic for later study. The following sections describe how to obtain printed schematics.

2. Set up *Design Architect* for printing
   First review the material in the **Getting Started** document on Generating Hardcopy, which introduces some general concepts.

   In order to set up *Design Architect* for printing, give the command: **(menu bar) MGC > Setup > Printer**. When the Setup Printer dialogue appears, enter the Printer name in the corresponding text box. Normally this will be **mgcps_a4**. Leave the number of copies set at 1 - the utility **mgcplot** will provide a means for printing a copy for each team member. Check that the Object Type is set to

Design, and that Scale is set to Fill Page. Orientation should be set to Best Fit; you may ignore the Panel Name box and the Priority and Notification settings. OK the dialogue.

3. Issue the Print Sheet command
   In order to print the sheet, give the command **(menu bar) File > Print Sheet:** When the Print Object prompt bar appears, verify that it contains the correct printer name, and correct if necessary. OK the prompt bar. A status message should confirm that operation has been successful.

4. Preview and print the resultant output
   As discussed in the introductory document, a special procedure is required to send the resultant postscript file to a suitable printing device. This is accomplished with a local utility, **mgcplot**. Open a new X terminal window, and when the Unix prompt appears, give the command: **mgcplot**. For the moment, press **Enter** when asked if you wish to process colour or A3 plots. Examine the list of output files you have so far generated, and select one by number. **Mgcplot** will now prompt you with a numbered list of output possibilities, including a Preview to Screen. You are recommended to use this to verify the results before committing them to paper. When you are ready, exit the **ghostview** Preview utility, and choose a printer if appropriate.

   You can defer printing until a later session if you prefer. However, note that you must run **mgcplot** on the same server as that which was used to give the **Print Sheet** command in paragraph 4.

Note: Unless you hear to the contrary, only the A4/monochrome printing options are available.

The remainder of the work in this Lab Guide consists of design exercises and should be completed away from the workstation.

Section II - Determination of Design Parameters

Exercises (to be completed away from the workstation)

The principles of the design of simple logic gates using MOS transistors have been covered briefly in the introductory lecture and in the pamphlet **Logic gates in CMOS**. You are now asked to explore how these principles apply to the detailed design of the two input NOR gate. The information gathered in the following sections will form an important contribution to the **First Interim Report**.

Use a printed copy of the nor2t schematic for the following exercises.

Exercise 1

- Determine the function of the ports A, B and Y.
- Identify the two different polarities of transistor, annotating your copy.
- Identify also the electrodes G, D and S on each transistor and annotate your schematic accordingly.
- What is the significance of the fourth electrode shown on each transistor, and why are they connected as shown?

Exercise 2

Construct a table indicating the state of conduction or non-conduction for each transistor with every possible combination of logic inputs, using the normal convention that logic 0 corresponds to 0 V, and logic 1 corresponds to 5 V.

Hence confirm the logical function of the gate.

What further information is required to determine the transfer function of the gate (i.e output voltage as a function of input voltage)?

Exercise 3

Some simple rules of thumb were given in the introductory lecture concerning MOS transistor channel conductances. The dimensions of the two transistors connected to ground are shown (units are micrometres). Using the process information appended to this sheet, determine the *approximate* conductance of each of these devices when conductive.

Exercise 4

Assume that the drain electrodes and associated interconnect linked to the output terminal of the **nor2** gate can be represented by a capacitance of 0.1pF (we shall determine this value much more accurately in a later section). Hence, using the simple approximations given in the lecture, deduce the approximate delay before the output terminal falls to logic 0 when:

- one input is brought abruptly to logic 1
  (does it matter which input? Explain, qualitatively);
- both inputs are brought abruptly and simultaneously to logic 1.

Exercise 5

Now consider the remaining two transistors, whose dimensions are not specified. These are to be chosen such that the output delay observed when both inputs are brought abruptly to logic 0 (i.e. for a *rising* output) matches the *falling* delay when a single input is brought to logic 1 - see Exercise 4.

Using the **Mietec CMOS24 process information** appended, which includes numerical values for the mobility μ for n and p-type devices, determine plausible values for the W dimension of these transistors, assuming that L is fixed at 3μm for all transistors. Where appropriate, refer also to the data supplied for the **Mietec NOR2** gate.

Exercise 6

Discuss briefly what determines the magnitude of the current drawn from the power supply (represented by a voltage source 5V). How does this depend on:

- the precise voltage at the inputs?
- the nature of the input waveform?

Using the concepts introduced in **Logic gates in CMOS**, estimate the *worst-case* current consumption for a single gate of this specification if it were to be used in your **ringarray** design. Assume for the moment that the gate output is a regular pulse train of period 50 ns (but note that your actual design may operate at a different frequency). You will have to make reasonable assumptions about other circuit parameters, which you should attempt to deduce from the information supplied. State any assumptions you make.

To what power dissipation does this correspond? What would be the current and power consumption of an integrated circuit consisting of 100,000 gates* of these characteristics, all operating under the same conditions? Comment!

*Note that this corresponds to about 400,000 transistors, representing a comparatively simple circuit compared with, say, the Intel Pentium which has upwards of 6 million transistors! However, in such a device as the Pentium, only a proportion of the devices would be configured as combinational gates.

Mietec CMOS24 process information

The IC process **CMOS24** employed in this project is supplied by Mietec-Alcatel. It defines a CMOS technology comprising p- and n- channel devices, which may be designed with channel lengths L of 3 μm minimum, and channel widths W also 3 μm minimum. These minimum dimensions represent a simple example of *design rules*, a collection of critical measurements and other constraints that must be satisfied by any IC layout if it is to be manufactured. The juxtaposition of layers required to form transistors will be described briefly in a lecture, and some details of the Mietec design rules will also be discussed.

The CMOS24 process offers two separate layers of metallisation (METAL1 and METAL2) to simplify layout of complex interconnections. In addition, the process provides for two separate layers of polysilicon (POLY1 and POLY2). POLY1 is used to fabricate the MOSFET gate electrodes, and it can also be used as interconnect for signals over short distances - say, 20 μm. Special structures known as *vias* (conceptually similar to plated-thru holes in PCBs) are used to make connections between layers. POLY2 is used primarily for implementing high value parallel-plate capacitors, and will not be mentioned further. The availability of two metal interconnect layers, plus polysilicon gives a topological freedom rather greater than that found with two layer printed circuit board technology. The Mietec process has design rules for metal and polysilicon interconnect layers, and for vias; these broadly specify layer widths and spacings which ensure that with expected processing tolerances, tracks are guaranteed to be conductive (no breaks) and adjacent tracks will not short-circuit.

The fundamental electrical characteristics of the process are given below. More complete details are available in the lab if needed.

Supply rail voltage	V_{dd}	5 volts
Mobility	μ_p	0.023 $m^2V^{-1}s^{-1}$
	μ_n	0.061 $m^2V^{-1}s^{-1}$
Gate capacitance per unit area	C_{ox}	8.2×10^{-4} F m^{-2} = 0.82 fF/μm^2
Gate oxide thickness	t_{ox}	40×10^{-9} m
Threshold voltage	V_{Tn}	+0.9 V
	V_{Tp}	-0.85 V
Interconnect capacitance per unit area		
metal 1 - substrate	C_{m1}	0.02 fF/μm^2
polysilicon-substrate	C_p	0.045 fF/μm^2
Interconnect sheet resistance		
metal 1	R_{m1}	25×10^{-3} Ω/square
polysilicon	R_p	23 Ω/square

Section III - Adaptation of the nor2t schematic

This part of the laboratory guide returns to the use of the Mentor Graphics *Design Architect* application in the capture and modification of transistor level schematics for the 2-input NOR gate which will later be designed as a mask layout. Correct transistor-level schematics are required for two main reasons:

- For comparison against the layout to check its correctness (LVS)
- To receive the *back-annotation* data obtained from the layout in the form of parasitic capacitances, for the purposes of detailed simulation with *AccuSim*.

When you complete this short session, you will have successfully adapted the **nor2t** schematic supplied part-completed for use in later simulation phases. You can carry out this activity at any time, but be sure to read the notes below which inform you of important actions which must be carried out before you start.

Important
Before you begin this section, you should be sure you understand the simple treatment of delays in CMOS logic gates and the simple techniques for obtaining equalised worst-case delays by attention to transistor channel dimensions (W/L) covered in the pamphlet **Design of logic gates in CMOS**. You should have studied the schematic and Mietec process information in **Laboratory Guide 3, Section B – Determination of design parameters**, and you should have carried out exercises 1-6 above.

You should not begin this session until you have attended to these points.

To begin, you should be logged in at a workstation as described in the **Getting Started** pamphlet, with *Design Manager* running. The current **Mentor Working Directory** should be **$CBT_WD.** *Design Architect* should also be running, but with no schematic or symbol window open.

1. Open the existing sheet **nor2t**.
   Click on the **OPEN SHEET** button in the palette window. The Open Sheet dialogue box appears.
   Fill in the Component Name box with: **$CBT_WD/nor2t**.
   Leave the sheet name as **sheet1** and OK the dialogue box.

2. Edit the **MODEL** properties of the four MOS transistors.
   As supplied, the **nor2t** schematic contains insufficient information about the electrical characteristics of the transistors for successful simulation of the device's behaviour using *AccuSim*. Channel width and length dimensions are incomplete; moreover, there is no indication of the physical characteristics of the devices - for example, the channel mobility, specific capacitances, etc. This information is provided in a set of technology files, normally by the manufacturer, and it is necessary to identify in the schematic a model name by which the required parameters can be accessed.

   In the Mietec process, n- and p-type transistors have model names: **tr_n** and **tr_p**.

   Use the command: **(Menu bar) > Edit > Edit commands > Properties > Change Text Values** - or any equivalent technique - to change the model name for each transistor to the correct value.

3. Edit the **INSTPAR** property.
   AccuSim requires information from the schematic about the dimensions L and W of each MOS transistor, which it obtains from the **INSTPAR** property. If this information is not given explicitly, the transistor channels are assumed by *AccuSim* to have dimensions 1m × 1m. The **INSTPAR** property is of the form:

   `L=xU W=yU`

   where *x* and *y* are suitable dimensions (basic units are metres) and the suffix U represents a multiplier of 10^{-6}. Use an appropriate property editing command to change the value of these properties to the values you calculated in the Exercises of Lab Guide 2a.

4. Check the resulting schematic visually, and confirm that the connections, models and properties are correct. In later lab sessions you will rely on the correctness of this schematic and its properties in a procedure which *verifies* the characteristics of an IC mask layout, so it is vital that it contain no errors or omissions.
   Use the appropriate *Design Architect* command to perform a syntax check on the sheet (but bear in mind that it will not warn you of incorrect model names or ridiculous dimensions). Save the modified **nor2t** schematic. Generate a hard copy using the procedure outlined earlier.

For the time being this completes the work required on the transistor-level specification of the 2-input NOR gate. We shall return to this when we consider how to design the physical layout of the 2-input NOR gate, for the purposes of comparison and simulation using *ICtrace*, *ICextract* and the *AccuSim* simulator.

First interim report

The first interim report will comprise the formal specification for the **ringarray** ring oscillator integrated design. You should therefore be sure you have read and understood the foundation material in the introductory sheets, and that you are confident you know what the basic design criteria are. The report should also include:

- the results of VHDL modelling (described in **Lab Guide 2**),
- exercises in pamphlet: **Design of logic gates in CMOS** & **Lab Guide 3** (above),
- annotated printouts of the transistor-level schematics produced so far, printed using the procedure introduced in this Guide.

The information gathered while carrying out Lab sessions 1, 2 and 3 should be of considerable help in compiling your report.

Please note that full digital schematics (described in **Lab Guide 4**) and material on **QuickSimII** digital simulation (described in **Lab Guide 5**) should be kept for the Second Interim Report.

Please refer to the project Web Page to access the latest information about recommendations for the first interim report.