Computer-Based Project in VLSI Design Co 3/7

Laboratory Guide 6 - IC layout with *ICgraph*

This laboratory guide provides an introduction to full-custom IC layout using Mentor Graphics' *ICgraph* tool, which forms a part of the *ICstation* package. The exercises in this session will lead to the creation of a layout for the 2-input NOR gate **nor2** which we shall substitute in place of the Mietec library version of that gate. The ultimate objective will be to obtain a neat, compact layout, free from design rule violations, with the fastest possible rise and fall times at the output terminal.

The starting point is a part-complete version of the required **nor2** layout. This is provided in your ~/cbt directory, and a plot is attached as an appendix to this guide. The layout supplied determines certain key aspects of the design - for example, the pitch between the metal interconnect lines corresponding to the supply rails, and the positions of the two inputs and the output - to ensure compatibility with other gates and cells used in the design. However, as provided, the **nor2** layout has no polysilicon transistor gate electrodes and some interconnect is omitted. In the later sections, you will remedy these omissions, adapt and enhance the design, and check that the resultant layout does not violate the applicable design rules. Before you begin, however, you should carry out the following preparatory exercises. You should include the resulting material in your final report.

The following activities do not require the use of the workstation. You need to complete these before you commence work on IC layout.

Consider the **nor2t** transistor level schematic studied in Lab Session 2. Use it to construct a simple stick diagram for the **nor2** gate, in the manner shown in the lecture. Compare your diagram with the given **nor2** layout, and determine the information listed below.

- Identify the positions of the various input and output ports on the layout.
- Determine the position of the supply rails, and use the ruler to measure their width and separation. What governs the width of the metal traces used for power supplies?
- The supplied **nor2** layout does not indicate the position of the gate, source and drain electrodes for the various transistors. Study the **nor2t** schematic and the **nor2** layout, and, taking into account the required transistor dimensions, attempt to determine the most suitable positions for these electrodes. You may find it helpful to refer to the notes on IC Layout and Symbolic Representation. Note also that there is no unique answer to this question, as a number of different possible layout styles are likely to be suitable.
- Annotate the **nor2** layout provided with the intended source and drain positions, and the sites where the polysilicon gate electrodes are required.
- Consider how to modify the layout to implement an electrical connection between the drain electrodes you have proposed, and the output port Y of the gate.

Discuss your conclusions briefly with a demonstrator.

In the following activity, you will modify the part-completed nor2 layout to make it suitable for incorporation into your ring design.

You should be logged in at a workstation as described in the **Getting Started** pamphlet, with *Design Manager* running. The current Mentor working directory should be **$CBT_WD** (which is the soft prefix for your $HOME/cbt directory), and you should select that same directory with the Navigator. An incomplete layout for the **nor2** cell is provided in that directory.

1. Open *ICgraph* on the cell **nor2**.
   The characteristic IC cell icon for the design **nor2** should be visible in the Navigator window. Select this icon, and use the *Data-Centred* mode of invocation to start up *ICgraph*: press the right (Menu) mouse button with the cursor over the Navigator window, and select the **Open** option in the menu that results; note that **ic** (for *ICgraph*) and **iclink** are the only tools eligible to be used with this type of object. Choose **ic**, and when the *ICgraph* design window appears, drag and adjust it as necessary to fill the screen. Examine the *ICgraph* session window.

2. Add two rulers to the layout to assist in sizing and placing objects.
   The partial cell design as supplied has a coordinate origin at the lower left corner: note the cross symbol which signifies this. Give the command:
   (Menu bar) > Objects > Add > Ruler.
   When the prompt bar appears, leave the settings at their defaults. Observing the cursor coordinates provided on the status bar, place the cursor at a horizontal coordinate of 0, and a vertical coordinate of around -5. At these coordinates, press and hold down the Select mouse button, and drag the resultant line horizontally to the right until it reaches a horizontal coordinate of 60 or so. Repeat this operation, but this time create a ruler starting at (-5,0) and extending vertically for the height of the design.

   If you make a mistake creating a ruler, use the command:
   (Menu bar) > Edit > Delete > Ruler.
   This will pop-up a prompt box that will allow you to click in the offending ruler and remove it.

3. Reserve the cell for Edit operations.
   Experimentally give the command: **(Menu bar) > Edit** in order to see the **Edit** menu. Note that at this stage virtually all the commands are greyed and unavailable. In fact, ***all*** commands for editing or changing the cell are disabled until an operation known as *reserving the cell for edits* is carried out. Since Mentor Graphics is a multi-user system, the possibility of two designers simultaneously attempting to edit a design must be avoided. Once a cell has been reserved by one designer, it cannot be reserved by any other user (or even the same designer in a separate **ic** session) until the original edit reservation is cancelled. In effect, cells are 'read-only' unless reserved for edit; then they become 'read-write'.

   In this project, each **mentor***x* user has a private copy of the original **nor2** cell.

   To reserve your private copy for edits, give the following command:
   (Menu bar) > File > Cell > Reserve > Current context.

4. Change the **Visible Layers** seen on the screen.
   Examining the **nor2** layout shows that it consists of a number of colour coded superimposed shapes or layers. As explained, the masks used in the various stages of the fabrication procedure are each represented by a colour-coded set of shapes. For the purposes of carrying out the design, it is vital to be able to visualise the complete mask set, to ensure that each mask is consistent with the remainder. However, this can lead to a rather complex cluttered appearance. Moreover, there are a number of layers which have significance to other parts of the design process but do not represent masks. Sometimes it is helpful to suppress display of certain kinds of shapes.

   For example, the entire **nor2** cell appears to be covered with hatched blue shapes which may impede visualisation of the design. These shapes are actually formed of two design layers: firstly, the mask for the **METAL1** aluminium interconnect used to interconnect devices; secondly, a layer which signifies to the automatic routing tool (to be explored later) regions in which **METAL1** may *not* be routed - referred to as **METAL1 blockage**. This second layer is not a mask layer, and it may enhance visibility of the design to suppress displaying the corresponding shapes.

   To experiment with this capability of *ICgraph*, give the following command: **(Menu bar) > View > Visible Layers**. This should result in the **Set Visible Layers** dialogue box being displayed. Using the scroll bars, scroll up and down the list, to get an impression of the kinds of layers available in this design, and how they look.

   Set the **Action** switch in the dialogue box to **Remove**, and select the **METAL1.BLKG** layer. OK the dialogue box,and study the resulting layout. Note that this has not changed the design in any way; it has simply made parts of it invisible.

   Using the same dialogue box, set the **Action** switch to **Replace**, and select the three layers: **METAL1**, **CONTACT**, and **POLY1**. You will need to hold down the **Ctrl** key while selecting the second and third layer. OK the dialogue box, and note that the resultant display is considerably simpler: only conducting (as opposed to semi-conducting) layers are now visible.

   Restore display of all layers by setting the **Action** switch of the **Set Visible Layers** dialogue box to **Replace**, and entering **All** in the **And/Or type in layers** text box, and finally OK the dialogue box.

   You may find it convenient to restrict visibility of the layers in the way just explored while carrying out the modifications described below.

5. Investigate the basic commands for placing shapes.
   Experiment with the keystroke commands **+**, **-** (on the Numeric Keypad) and **Shift+F8**, which control the display zoom factor. Zoom the display so that there is a substantial clear region to left and right of the **nor2** structure.

   Give the command: **(Menu Bar) > Objects > Add > Shape**. This allows you to add a rectangle or polygonal shape to the layout. When the prompt bar appears, click the **Options** button, and select **POLY1** in the scrolling list of layer names that appears. Check the **Keep Option Settings** button, and OK the Options dialogue box. Now, with the cursor over a clear area of the design window, and with the Select mouse button depressed, drag out a rectangle. Observe that the size of the rectangle is read out in the status bar. Release the button when the

rectangle is about 40 μm square, and observe that it is displayed *selected*, in bold, dashed red. Observe also the bold white **I** at one corner of the shape. This is the *basepoint*. When you **Copy** or **Move** selected objects, they are placed so that when you identify the destination point with the mouse, the basepoint is placed here, and all other elements of the selection are placed relative to it.
Experiment with **(Menu bar) > Edit > Move** and **(Menu bar) > Edit > Copy**, **(Menu bar) > Edit > Flip** and **(Menu bar) > Edit > Rotate**, using them to move your shape to a different position, manipulate it, and create a duplicate.
When you finish with these commands, press **F2** to de-select all objects.

Repeat the **(Menu Bar) > Objects > Add > Shape** command, leaving the options at their defaults. However, on this occasion, instead of dragging out a rectangle, define a closed polygon in the shape of a **T** - in a clear area of the design, by clicking the Select button at its vertices and double-clicking at the end point (which should coincide with the start point). The shape outlined should be displayed, selected, as polysilicon.

6. Investigate the Notch and Stretch commands for editing shapes.
First investigate the **Notch** command. De-select all shapes by pressing **F2**. Select just one of your shapes by clicking it. Give the **(Menu bar) > Edit > Notch** command. When the prompt bar appears, place the cursor within your shape, and using the Select button, drag out a rectangular region which extends outside the shape. Release the Select button. Observe the results.
Repeat the command, but on this occasion begin dragging outside your shape and allow the rectangle being dragged out to enter the shape. Experiment further with this command if you wish.

   Now investigate the **Stretch** command. Ensure just one of your shapes is selected, and give the command: **(Menu bar) > Edit > Stretch**. Drag out a rectangle (using the Select button) which fully encloses *one* edge of the selected shape. The white rectangle should persist; now drag out a line starting at a point within the white rectangle, and roughly perpendicular to the chosen edge, and finishing outside the box. Release the Select button, and observe the results. Experiment further with **Stretch** if you wish.

   Now delete the two experimental shapes you have created by selecting them (only), and using the **(IC Window) > Edit > Delete** command.

   In order to ensure you start with a clean copy of **nor2**, close the cell now by double clicking the system button at the top left of the design window. When the dialog box: **Save changes to nor2 ?** appears, click the **Discard** button and OK the box. Re-open the **nor2** cell by giving the command:
(Menu bar) > Open > Cell,
and navigate to the **nor2** design if necessary. Reserve the cell for edits.

7. Run *ICrules* to check for any existing design rule violations
The importance of ensuring that any mask layout comply with the manufacturer's design rules has been mentioned. When a layout is being edited manually, it is necessary periodically to run a check that none of the shapes laid down violates the set of rules. This is done by means of *ICrules*, an interactive tool controlled from within *ICgraph*, which detects and highlights any rule violations. *ICrules* is a complex application in its own right, with a large number of options and facilities. However, our use of it will be comparatively straightforward.

As provided, the **nor2** cell has some design rule violations which you are asked to identify and correct. To run the design rule check (DRC), click the **ICrules** entry in the IC palette, which switches to display a different palette, that for *ICrules* itself. The **nor2** design is automatically set up to use the correct rule set (Mietec CMOS24).

To begin the check, click the **Check** palette menu item, and note that a prompt bar appears. You can investigate the options by clicking the appropriate button, but leave them at their defaults. You can further optionally specify a rectangular area (using the mouse select button to drag out an area) in which the check is to be confined. In this case we shall leave the area unspecified, causing *ICrules* to check the entire design. OK the prompt bar and observe the status line.

You may observe some warning messages flash past. When the check is complete, any warnings or errors are gathered into a database. Access the first by clicking the **First** item in the palette. You should observe a portion of the design flash three times, then remain illuminated. This identifies the site of the error. The description is presented in the status line. Study the layout and the error description carefully, and try to identify the correction(s) required. Consult a demonstrator if you are unsure. When you have made the necessary change, you can move to the next violation by clicking the **Next** item. When you have corrected all problems in this way, re-check the design once again. You need to aim for a clean DRC, in which the report: **Total results: 0** will be seen at the foot of the screen.

When you achieve this, save the cell by giving the command:
(Menu bar) > File > Cell > Save Cell.
Note that the act of saving the cell also removes the edit reservation. In order to continue editing the cell after each **Save**, you will need to reserve it for editing once again.

8. Lay out the gate electrode for input **A**.
   Referring to your stick diagram and annotated layout, decide where to place the polysilicon gates to form the n- and p-type transistors required in the **nor2** design to connect to input **A** (at the base of the design). Broadly speaking, you need to create a set of vertical strips - though not necessarily of uniform width or in straight lines - connected to the corresponding input port and crossing two active regions. Be careful that the layout you choose will not impede you in designing a similar structure for input **B**.

   Use the **(Menu bar) > Objects > Add > Shape** command investigated above to generate the gate connected to input port **A**. You may have to do this in a number of stages, using abutted or overlapped rectangles of different sizes. Use *ICrules* at frequent intervals to verify that the structures you design are free from violations. Although this may seem irksome, it is probably more efficient in the long run than laying down an entire complex structure and having to wade through a plethora of violation messages at the end. The demonstrators will help you interpret any less obvious warning/error messages.

9. Lay out the gate electrode for input B.

   Referring to your stick diagram and annotated layout, decide now where to place the polysilicon gates corresponding to input **B** (at the base of the design). Again, a vertically oriented strip of polysilicon is likely to be required. On this occasion, instead of laying out a set of abutting shapes, we shall use *ICgraph*'s facility for laying out **path** structures. With this command, you determine the position of the centre line of a rectangular shape, which may have jogs and changes of direction if required; software then 'fleshes out' the centre line to the required width. **Path** structures can as a result be recognised by the existence of a prominent centre line.

   Determine a suitable width for the path, noting that this will be constant over the whole of its length. Give the command: **(Menu bar) > Objects > Add > Path**. When the prompt bar appears, click the **Options** button and examine the dialogue box that results. Select **POLY1** as the layer name for the path, and enter the value you have chosen for its width (in μm). OK the dialogue box. Using the Select button, mark the position of the start point and, in order, any other vertices required, double clicking at the end point. The path will then be displayed, filled out to the prescribed width, and selected.

   If you are unhappy with the course of the path, perhaps because it violates a design rule, or for any other reason, you may delete it like any other shape. Alternatively, you can use **Stretch** to extend a segment. Note that you can also select a segment of the **path** itself, by giving the command:
   (Menu bar) > Select > Select > Edge:, then clicking the Select button with the cursor over the centre of the segment in question.
   The **(Menu bar) > Edit > Move** command may then be used to reposition the path as required. Alternatively, with the whole of the path selected, you can use **(Menu bar) > Edit > Edit Ctrline** to continue the path. When you are satisfied, check that *ICrules* runs clean, save the design and reserve it for further edits.

   Take great care that your polysilicon gate electrodes have the correct dimensions so they correctly define the length of the conductive channel. They must of course satisfy the design rule requirements, but you will only achieve the anticipated electrical performance if the transistor dimensions are chosen correctly and laid out in accordance with your earlier calculations. Edit if necessary.

10. Insert interconnect to link the output port

    The output port **Y** (at the base of the cell) marked on the layout **nor2** is not physically connected to any of the semiconductor devices of the NOR gate. As shown in the earlier exercise, additional interconnect is required to achieve this. Study the layout and schematic carefully, and check the viability of your proposed scheme for linking the points in question. You may need to investigate carefully what layers already exist at and around the two points, changing the **Visible Layers** setting in order to confirm matters where there is any uncertainty. Note that any additional structures you create must not stray outside the white rectangular **floorplan** boundary (layer **fp1**). If you are in doubt about the options available, consult a demonstrator.

    Use either the **.. Add > Shape** or the **.. Add > Path** command to add appropriate shapes or paths to achieve the required linkage. As always, use *ICrules* to check for design rule violations, and when you are content with the result, save the cell.

11. You will probably wish to generate a checkplot of your completed **nor2** layout. At this stage a monochrome laser printout should serve your needs, but you may wish to annotate or colour code the result for inclusion in your report in the interests of clarity. The procedure for generating hardcopy of layout files resembles that for schematics and waveforms, but with a few important differences. Follow the procedure set out below.

    Give the command: **(Menu bar) > MGC > Setup > Printer...** When the **Setup Printer - General** dialogue box appears, enter `mgcps_a4` in the **Printer Name** field. Check that the **Object type** is set to **design** (correct if necessary). Leave the remaining fields in their default states, and OK the dialogue box.

    In order to print the cell, you must have it visible on the screen, and the design window must be active.

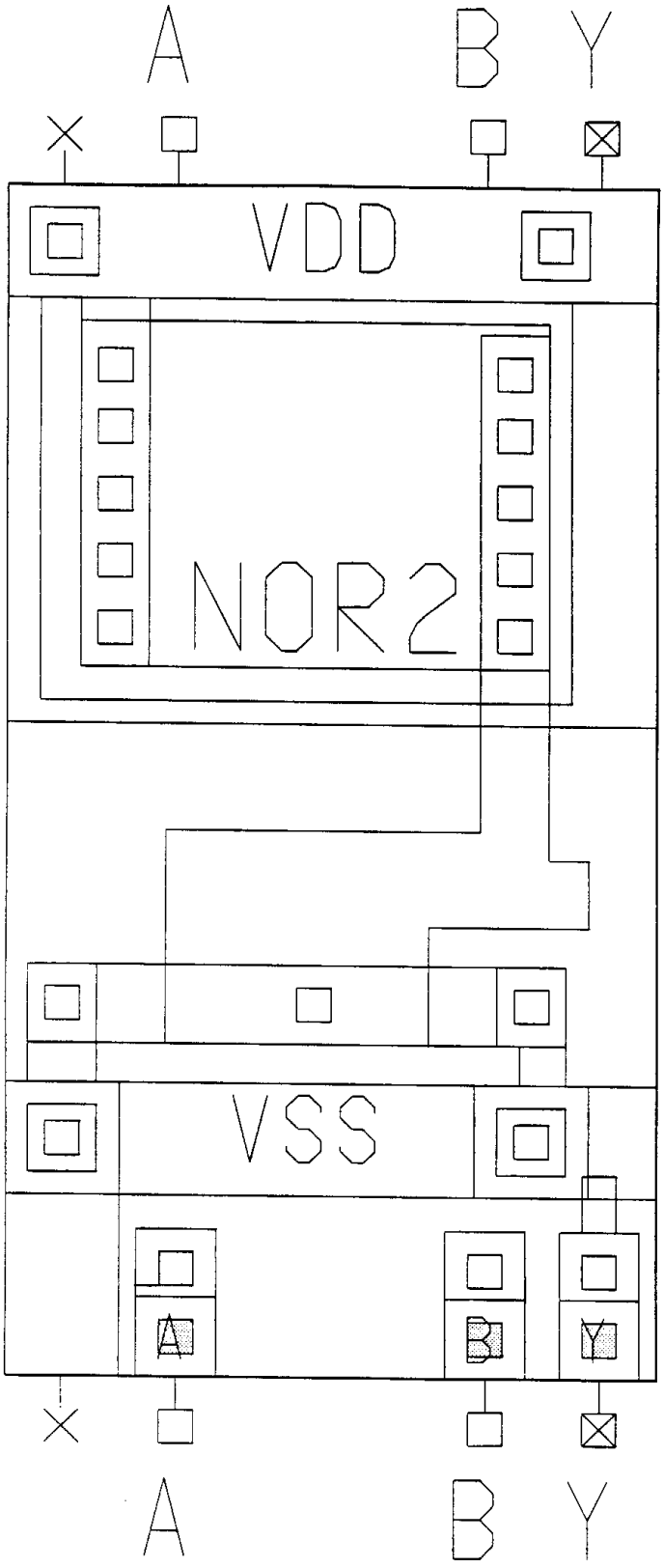
    Give the command: **(Menu bar) > File > Print > Print Cell ...** When the **Print Cell** dialogue box appears, first click the **Setup Print...** button. A further, **Setup Print** dialogue box appears. In this box set the **Paper Width** to 7 inches and the **Paper Length** to 10 inches. Leave the other settings at their default values and OK the dialogue box.

    When the **Print Cell** dialogue is revealed again, you must enter again the parameters for the paper to be used. Enter **7** in the **Wid** field, and **10** in the **Len** field. Units are inches in both cases. Now click the **Set** button just below the **Len** entry field. Click in sequence the **Set** buttons to the right of the **Pages** and the **Scale** fields.

    Finally, click the **Set Layers** button. You are strongly advised to suppress printing of the **Metal1.blkg** and **Metal2.blkg** layers, since these occupy much of the layout and are shown as a strongly hatched design on the plot, obscuring much of the detail below. To achieve this, you must select the list of layers you **do** wish to see, and ensure that this does not include the unwanted blockages. Starting at the top of the list in the scrolling box, click the layers down to number 13, pressing the **Shift** key while you click, so as to obtain an additive selection. Select also any other layers you particularly wish to include. When you have finished selecting layers, OK the dialogue, and note that the **Layers** item is now set to **Other** in the **Print Cell** dialogue box. OK the **Print Cell** dialogue.

    The plot will then be prepared and placed in a temporary directory. To send it to the laser printer, run the utility **mgcplot** from an **xterm** shell or similar. The name of the cell you plotted should then be listed. Follow the screen prompts to preview the plot (using **ghostview**) before committing it to paper. When you are happy with the result, exit from **ghostview** and follow the prompts to direct the output to the laser printer.

    A similar procedure will be required in the final lab session, in which you will plot the layout corresponding to the entire design, including input/output pads and all other essential elements. At that stage it is anticipated that colour printing facilities should be available, but note that a slightly different procedure is required to obtain colour prints.



Layout of **nor2** cell before modification
Dimensions of the rectangular bounding box are 106 μm × 57 μm